

09915792_CLS
Most Frequently Occurring Classifications of Patents Returned
From A Search of 09915792 on October 28, 2003

Original Classifications

4	326/93
4	716/17
3	716/8
2	365/200
2	716/10
2	716/11
2	716/12
2	716/6
2	716/9

Cross-Reference Classifications

5	716/16
5	716/18
5	716/6
3	257/211
3	716/10
3	716/2
3	716/8
3	716/9
2	257/205
2	257/208
2	257/E23.151
2	257/E27.106
2	326/21
2	370/517
2	716/1
2	716/14
2	716/17

Combined Classifications

7	716/6
6	716/16
6	716/17
6	716/8
5	716/10
5	716/18
5	716/9
4	326/93
3	257/211
3	716/11
3	716/12
3	716/2
2	257/205

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2 257/207
2 257/208
2 257/E23.151
2 257/E27.106
2 326/21
2 365/200
2 365/230.05
2 370/517
2 375/376
2 714/724
2 716/1
2 716/14
2 716/3
2 716/4
2 716/5

09915792_CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 09915792 on October 28, 2003

7	716/6	(2 OR, 5 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/4	.Testing or evaluating
	716/5	..Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width)
	716/6	...Timing analysis (e.g., delay time, path delay, latch timing)
6	716/16	(1 OR, 5 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/12	.Routing (e.g., routing map, netlisting)
	716/16	..PLA, PLD, FPGA, OR MCM
6	716/17	(4 OR, 2 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/17	.Programmable integrated circuit (e.g., basic cell, standard cell, macrocell)
6	716/8	(3 OR, 3 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/8	.Floorplanning
5	716/10	(2 OR, 3 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/8	.Floorplanning
	716/10	..Constraint-based placement (e.g., critical block assignment, delay limits, wiring capacitance)
5	716/18	(0 OR, 5 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF CIRCUIT OR SEMICONDUCTOR MASK

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716/1      CIRCUIT DESIGN
716/18     .Logical circuit synthesizer

5  716/9      (2 OR, 3 XR)
    Class    716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                  CIRCUIT OR SEMICONDUCTOR MASK
716/1      CIRCUIT DESIGN
716/8      .Floorplanning
716/9      ..Detailed placement (i.e., iterative
                  improvement)

4  326/93     (4 OR, 0 XR)
    Class    326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/93     CLOCKING OR SYNCHRONIZING OF LOGIC STAGES OR
                  GATES

3  257/211    (0 OR, 3 XR)
    Class    257 : ACTIVE SOLID-STATE DEVICES
257/202    GATE ARRAYS
257/208    .With particular signal path connections
257/211    ..Multi-level metallization

3  716/11     (2 OR, 1 XR)
    Class    716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                  CIRCUIT OR SEMICONDUCTOR MASK
716/1      CIRCUIT DESIGN
716/8      .Floorplanning
716/11     ..Layout editor (e.g., updating)

3  716/12     (2 OR, 1 XR)
    Class    716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                  CIRCUIT OR SEMICONDUCTOR MASK
716/1      CIRCUIT DESIGN
716/12     .Routing (e.g., routing map, netlisting)

3  716/2      (0 OR, 3 XR)
    Class    716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
                  CIRCUIT OR SEMICONDUCTOR MASK
716/1      CIRCUIT DESIGN
716/2      .Optimization (e.g., redundancy, compaction)

2  257/205    (0 OR, 2 XR)
    Class    257 : ACTIVE SOLID-STATE DEVICES
257/202    GATE ARRAYS
257/204    .Having specific type of active device (e.g.,
                  CMOS)
257/205    ..With bipolar transistors or with FETs of onl

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ement-depletion
one channel conductivity type (e.g., enhanc
FETs)

2 257/207 (1 OR, 1 XR)

Class 257 : ACTIVE SOLID-STATE DEVICES

257/202 GATE ARRAYS

257/207 .With particular power supply distribution
means

2 257/208 (0 OR, 2 XR)

Class 257 : ACTIVE SOLID-STATE DEVICES

257/202 GATE ARRAYS

257/208 .With particular signal path connections

2 257/E23.151 (0 OR, 2 XR)

Class 257 : ACTIVE SOLID-STATE DEVICES

257/E23.139 ...Liquid at normal operating temperature of
device (EPO)

257/E23.141 .Arrangements for conducting electric current
within device in operation from one compo

nent to another,

interconnections, e.g., wires, lead frame

s (EPO)

257/E23.142 ..Including external interconnections

consisting of multilayer structure of cond

uctive and

insulating layers inseparably formed on se

miconductor body

(EPO)

257/E23.151 ...Geometry or layout of interconnection
structure (EPO)

2 257/E27.106 (0 OR, 2 XR)

Class 257 : ACTIVE SOLID-STATE DEVICES

257/E27.006 .Including piezo-electric, electro-resistive,
or magneto-resistive component (EPO)

257/E27.009 .Including semiconductor component with at
least one potential barrier or surface

barrier adapted
for

rectifying, oscillating, amplifying, or

switching, or

Including integrated passive circuit el

ements (EPO)

257/E27.01 ..With semiconductor substrate only (EPO)

257/E27.07 ...Including a plurality of individual
components in a repetitive configuration

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(EPO)

257/E27.105Masterslice integrated circuit (EPO)
 257/E27.106Using bipolar structure (EPO)

2 326/21 (0 OR, 2 XR)
 Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
 326/21 SIGNAL SENSITIVITY OR TRANSMISSION INTEGRITY

2 365/200 (2 OR, 0 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/189.01 READ/WRITE CIRCUIT
 365/200 .Bad bit

2 365/230.05 (1 OR, 1 XR)
 Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
 365/230.01 ADDRESSING
 365/230.05 .Multiple port access

2 370/517 (0 OR, 2 XR)
 Class 370 : MULTIPLEX COMMUNICATIONS
 370/473 ..Transmission of a single message having
 multiple packets
 370/498 .Combining or distributing information via tim
 e
 channels
 370/503 ..Synchronizing
 370/516 ...Adjusting for phase or jitter
 370/517Including delay device

2 375/376 (1 OR, 1 XR)
 Class 375 : PULSE OR DIGITAL COMMUNICATIONS
 375/354 SYNCHRONIZERS
 375/371 .Phase displacement, slip or jitter correction

 375/373 ..Phase locking
 375/376 ...Phase locked loop

2 714/724 (1 OR, 1 XR)
 Class 714 : ERROR DETECTION/CORRECTION AND FAULT
 DETECTION/RECOVERY
 714/699 PULSE OR DATA ERROR HANDLING
 714/724 .Digital logic testing

2 716/1 (0 OR, 2 XR)
 Class 716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
 CIRCUIT OR SEMICONDUCTOR MASK
 716/1 CIRCUIT DESIGN

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2	716/14	(0 OR, 2 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
		CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/12	.Routing (e.g., routing map, netlisting)
	716/14	..Detailed routing (e.g., channel routing, switch box routing)
2	716/3	(1 OR, 1 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
		CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/3	.Translation (e.g., conversion, equivalence)
2	716/4	(1 OR, 1 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
		CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/4	.Testing or evaluating
2	716/5	(1 OR, 1 XR)
	Class	716 : DATA PROCESSING: DESIGN AND ANALYSIS OF
		CIRCUIT OR SEMICONDUCTOR MASK
	716/1	CIRCUIT DESIGN
	716/4	.Testing or evaluating
	716/5	..Design verification (e.g., wiring line capacitance, fan-out checking, minimum path width)

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4878209 61
6418067 61
6120549 58
4482953 54
6195787 54
6182233 54
6216258 54
6216258 54
6243851 54
6260182 54
6292925 54
6457164 54
5870309 52
5949690 52
6446230 52
6012833 52
5565798 46
5708374 46
5475607 46
5737237 46
5835571 46
6151266 46
6166564 46
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4954953 46
5210699 46
5544203 46
5740412 46
5761078 46
5764532 46
5787092 46
5796662 46
5844954 46
5963730 46
5961653 46
5970052 46
6005416 46
6134704 46
6351170 46
6453258 46
6518793 46
6609241 46
5446675 45
6304998 45
5602406 44
5698876 44
6181634 44
4255672 44

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4278897 44
4849904 44

09915792 LIST

PLUS Search Results for S/N 09915792, Searched October 28, 2003

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6418067
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